Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHRISTIAN VAL,
YVES VAN CAMPENHOUT,
and DOMINIQUE GILET

Appeal No. 1999-0878
Application 08/182,093[1]

HEARD: April 3, 2001

Before BARRETT, FLEMING, and BARRY, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

[1] Application for patent filed January 25, 1994, entitled "Method For The Manufacturing Of A Semiconductor Device Which Comprises At Least One Chip And Corresponding Device," which is a national stage application under 35 U.S.C. § 371 of international application PCT/FR93/00513, filed May 26, 1993.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 14-16, 19-25, and 27-31.

We reverse.

BACKGROUND

The invention is directed to a semiconductor device which has a minimum size and which can be easily tested and inspected. Claim 22 is reproduced below. Claim 22 is broader than claim 14[2] because it does not contain the additional limitation of "a sloping side for facilitating visual inspection."

> 22. A semiconductor device having at least one chip including at least one connecting site, comprising:
>
> a first electrically insulating means directly coating a surface of the at least one chip;
>
> at least one electrical connection means penetrating the first electrically insulating means to contact the at least one connection site of the at least one chip and to connect the at least one connecting site of the at least one chip to a metallized contact means formed on an outside surface of said first electrically insulating means, wherein the at least one electrical connection lead is substantially perpendicular to both the at least one connection site of the at least one chip and the metallized contact means.

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[2] We note for the record that claim 14 is reproduced incorrectly in the appendix to the brief.

The Examiner relies on the following prior art:

Lee et al. (Lee) 4,667,219 May 19, 1987

Claims 14-16, 19-25, and 27-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee.

We refer to the final rejection (Paper No. 16) (pages referred to as "FR__") and the examiner's answer (Paper No. 24) (pages referred to as "EA__") for a statement of the Examiner's position, and to the appeal brief (Paper No. 23) (pages referred to as "Br__") and the reply brief (Paper No. 26) (pages referred to as "RBr__") for Appellants' arguments thereagainst.

OPINION

Initially, we agree with Appellants that the grounds of rejection contain several inconsistencies in reading the claims onto the elements of Lee. In the final rejection (FR2), the Examiner referred to both elements 80 and 18 in Lee as the insulating material, and found element 16 to be the chip. In the examiner's answer (EA3), the Examiner found element 80 to be the insulating material and referred to both elements 16 and 18 as the chip. As noted by Appellants (Br4; RBr2), element 18 is a semiconductor chip (col. 3, line 49),

not an insulating material formed on a chip, and element 16 is a cold plate of a heat sink 12 (col. 3, lines 15-17), not a chip. The Examiner should be more careful in stating the rejection since it is the examiner's final rejection that is being reviewed under 35 U.S.C. § 134, In re Webb, 916 F.2d 1553, 1556, 16 USPQ2d 1433, 1435 (Fed. Cir. 1990), and it may not be possible to "fix up" a poorly worded final rejection in the examiner's answer without creating an impermissible new ground of rejection under the new rules for examiner's answers. However, we think it is apparent here that, with reference to figure 8 of Lee, the Examiner intended chip 18 with contacts 44, 46, and 48 to correspond to the claimed "at least one chip having at least one connecting site"; the electrically insulating connector plate 80 to correspond to the "electrically insulating material" (claim 14) or the "electrically insulating means" (claim 22); and the S-shaped copper wires 84 to correspond to the "at least one electrical connection lead" (claim 14) or the "at least one electrical connection means" (claim 22).

The differences between Lee and the claimed subject matter are: (1) the electrically insulating connector

plate 80 is spaced from the surface of the chip and is not an "electrically insulating material directly coating a surface of the at least one chip" (emphasis added) (claim 14) or "electrically insulating means directly coating a surface of the at least one chip" (emphasis added) (claim 22); and (2) the ends of the S-shaped wires 84 pass through connector plate 80 and a solder connection is made to each power post 64, signal post 67, and ground post 72 (col. 4, line 67 to col. 5, line 1) and, thus, there is no "metallized contact formed on an outside surface of said first electrically insulating material" (claim 14) or "metallized contact means formed on an outside surface of said first electrically insulating means" (claim 22).

The Examiner concludes in the final rejection (FR2): "It would [have] be[en] considered obvious to one having ordinary skill in this art to form insulating layer 18 [sic, 80] directly on the surface [of] chip 16 [sic, 18] because insulating substrates [sic, layers?] formed directly on chip surfaces are not new in this art and are typically provided thereon."

This is a single reference § 103(a) rejection and, thus, it would be expected that the differences between Lee and the claimed subject matter are trivial and can be accounted for by minor obviousness reasoning based on the knowledge of those skilled in the art. That is not the case. The Examiner provides no factual evidence for the statement that "insulating substrates [sic, layers?] formed directly on chip surfaces are not new in this art and are typically provided thereon" (FR2). In effect, the Examiner takes Official Notice of this fact to avoid having to produce a reference. Official Notice should not be used except where the proposition at issue is supported by common knowledge or capable of unquestionable demonstration. See In re Knapp-Monarch Co., 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961). See also In re Cofer, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Cf. In re Eynde, 480 F.2d 1364, 1370, 178 USPQ 470, 474 (CCPA 1973) (court will not take judicial notice of the state of the art). "Assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art . . . ." In re Ahlert, 424 F.2d 1088, 1091, 165 USPQ 418,

420 (CCPA 1970); accord In re Pardo, 684 F.2d 912, 917, 214 USPQ 673, 677 (CCPA 1982). The fabrication of semiconductor devices is the kind of complex technology that does not lend itself to Official Notice. Neither we nor our reviewing court, the U.S. Court of Appeals for the Federal Circuit, have any way of reviewing the fact asserted by the Examiner. Even if insulating layers were well known in the semiconductor art, the Examiner provides no explanation of why one skilled in the art would have been motivated to use such insulating layers in Lee. The purpose of the connector plate 80 in Lee is to provide a flexible coupling between the chip contacts and the appropriate plate or signal lead (col. 6, lines 9-22), and forming the connector plate 80 directly on the surface of the chip 18, as proposed by the Examiner, would be directly contrary to this purpose. Accordingly, the Examiner has failed to establish a prima facie case of obviousness of the claimed insulating layer directly coating a surface of the chip.

Furthermore, the Examiner failed to address in the final rejection, and, thus, failed to establish a prima facie case of obviousness of, the limitation of the metallized contact

formed on an outside surface of the electrically insulating material.

In the examiner's answer, the Examiner provides the following new reasoning (EA4): "Further semiconductor chips develop native oxides on their surfaces so chip 18 would be deemed to posses [sic, possess] a native oxide (insulating) layer on its surface with said contact 86 penetrating therethrough." The Examiner also states (EA4): "Electrical insulating materials are grown on semiconductor chip[s] as native oxides[,] thus the chip of Lee is deemed to have one such oxide on its surface. Typical also in this art are metallized contacts such as Lee's 86 formed on chip surfaces and penetrating outside the surface of said native oxide."

We agree with Appellants' arguments that the basis for the rejection is not clear. The Examiner appears to shift from the proposed modification of moving insulating layer 80 onto the surface of the semiconductor chip 18, to a completely new inherency argument for the limitations in the chip 18 itself without reference to layer 80. No inherency has been factually established. If the Examiner wants to rely on the structure of a chip, then the Examiner should cite a reference

to a chip instead of just making unsupported assertions. Furthermore, the Examiner's reasoning fails to point out the location of the connecting site in Lee and how a connection lead would connect a metallized contact to such a connection site.

Because Lee does not disclose or suggest the limitations of (1) an insulating layer directly coating a surface of the chip, and (2) a metallized contact formed on an outside surface of the electrically insulating material, the Examiner has failed to establish a prima facie case of obviousness. Accordingly, the rejection of claims 14-16, 19-25, and 27-31 is reversed.

REVERSED

LEE E. BARRETT Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.
1755 Jefferson Davis Highway
Fourth Floor
Arlington, VA 22202